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PARALLEL FUNCTION PROCESSOR
HARDWARE OPERATION

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COMPUTER ENGINEERING RESEARCH LABORATORY

Georgia Institute of Technology

Atlanta, Georgia 30332 - 0540

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Author

Michael B. Woods

COMPUTER ENGINEERING RESEARCH LABORATORY

Georgia Institute of Technology

Atlanta, Georgia 30332-0540

Eugene L. Sanders
USASDC
Contract Monitor

Cecil O. Alford
Georgia Tech
Project Director

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1. Scope

1.1 Identification

This Computer System Operator's Manual (CSOM) applies to Georgia Tech's Parallel Function Processor (PFP), Georgia Tech part number CERL002-0757-000.0.

1.2 System Overview

The PFP is a 64 processor computing engine for use in computationally intensive applications that can be partitioned into functional blocks. The processors are grouped in two 32 processor clusters running from one common host. Each 32 processor cluster is connected by a crossbar switch. All inter-processor communication takes place over the crossbar(s). Simultaneous transfers may take place independently and switch patterns may be changed every cycle. In order to program the machine correctly, all inter-processor communication and data transfer lengths must be known beforehand.

The PFP has been designed to accomodate "hardware in the loop" simulations running in real time. Actual hardware components may first be simulated on one or more processors and later replaced with actual hardware interfaced to specified crossbar ports. The inputs and outputs to/from the device will appear identical to those it would see in an actual system.

1.3 Document Overview

The purpose of this manual is to give the reader a basic understanding of how the PFP works, its capabilities, and how to use it. The manual contains all instructions for operating the unit and a brief architectural overview. Refer to document #CERL002-0757-100.1 for detailed programming instructions.

2. Referenced Documents

PFP Programmer's Guide

PFP Technical Data Package

Intel System 310 Hardware Literature

Intel iRMX Operating System User's Manual

3. Computer System Operation

3.1 Computer System Preparation and Shutdown

3.1.1 Power On and Off

Power is supplied to the PFP through 7 separate AC power cables located at the bottom rear side of the unit. Each cable must be plugged into a circuit capable of supplying it 115V, 60 Hz, power at 15 amperes.

After the PFP has been plugged in, there are 7 circuit breakers located in the rear of the unit that must be turned on. An orange light next to each breaker indicates that it is on. See figure 3.1-1 for location of the breakers.

There are 7 power switches located on the front of the machine (See figure 3.1-2). Six of the switches turn on power to the processor racks. The seventh switch turns on power to the crossbars. Turn on all seven switches to activate full power to the unit.

The Intel 310 host may be powered on its own AC circuit or from the same circuit as the center rack. The power switch to the 310 is located on the rear side of the host case. Turn the switch to the on position to activate power to the host.

3.1.2 Initiation

After power up or system reset, the Intel 310 host automatically runs through self diagnostics and bootstrap program. The system then prompts the user to log on with the following prompt:

    LOGON:

The host is now initialized and ready to use.

On power up or system reset, each processor in the PFP automatically runs through self diagnostics. Each processor has 4 LEDS on the front to indicate status conditions. When the green LED is on and the other three are off, that processor has completed its self diagnostics. When all processors have completed their self diagnostics the system is ready to use.

The PFP does not run an operating system and does not require any special initialization. All programs are down loaded from the host as executable code and given a start command by the host. Data is read back by the host during program execution or after the program has finished.

3.1.3 Shutdown

Prior to shutting down the Intel 310 or the PFP, all data that may be needed later must be saved. Data on the PFP must be read by the host and saved on one of the host's storage media (i.e., tape, floppy, or hard disk). After data has been saved, the host is shut down by turning the power switch off located at the rear of the unit.

The PFP is shut down by turning the seven power switches off located on the front of the center rack on the PFP.

3.2 Operating Procedures

3.2.1 Input and Output Procedures

All input and output media for the PFP system are accessed through the host Intel 310. The host contains a 40 mb hard disk drive, a 360 kb floppy disk drive, and a 60 mb cartridge tape drive. The host runs Intel's iRMX I operating system. In order to store data generated by the PFP, it must be read by the host and then stored to the selected device using the appropriate iRMX system command. See Volume 4, "Operator's Guide to the Human Interface", of the iRMX I Operating System Manual for detailed instructions.

The host is set up as a single user system. All system prompts and messages appear at this console. After the host is powered up or the system is reset, the host will run through self diagnostics then come up with the log on prompt. To use the PFP in conjunction with the 310 host, enter the following responses:

```
LOGON:PFP

PASSWORD:PFP
```

To exit the system, type the command "logoff".

3.2.2 Monitoring Procedures

Write statements may be sent to the console screen to monitor the operation of software running on the host 310. If the host is running in conjunction with the PFP, it may be used to read data from the PFP and display it (or save it) while the program is executing.

The PFP has two devices for monitoring a program during execution, 1) the crossbar status displays and 2) the sequencer/processor transition boards. These displays are most valuable for debugging new application programs as they are being developed. The crossbar status display shows the current switch patterns set in the crossbar. When a program is executing properly, the display appears as a bunch of flickering lights. When the program stops or hangs up, it appears as a set of arrows on a rectangular grid showing which processors are sending on that cycle, which processors are receiving, and the data paths being used. Two displays exist in the front of the center rack of the system. The top display shows the crossbar patterns for the left bank of 32 processors. The bottom display shows the switch patterns for the right bank of 32 processors.

The sequencer/processor transition boards are located inside the rear doors of the two processor racks. Each board has LED's indicating the status of the four handshake lines coming from each processor. The four lines from each processor are DAV/ (data is available at the processor and ready to send to the network), ROT/ (read data out of the processor into the network), RFI/ (processor is ready for input from the network), and WIN/ (write data into the processor from the network). All lines are asserted low. An LED is off if the line is asserted and on if it is not. As with the crossbar display, the display appears as flickering lights during program execution. When a program hangs up, the lights can be used for program diagnosis.

The crossbar status display and sequencer/processor transition boards actually function as a pair when debugging a program. The crossbar status display allows the user to tell which program cycle the machine has stopped on. The sequencer/processor transition boards allow the user to tell which processor hung up the system on that cycle. That processor can then be interrogated by the host to determine its status. The code for that block can be modified to send more debug information to the host until the problem is resolved. Appendix B contains 3 example crossbar transfer cycles and the display patterns (both crossbar display and sequencer/processor transition boards) that go with them. Each example is explained in detail and should be read to learn what to look for on the displays.

3.2.3 Recovery Procedures

In the event the operation of the Intel host is interrupted or aborted, the system can be re-booted by pressing the button labeled "R" on the front lower left corner of the host case. The machine will run through its self diagnostics and come up with the logon prompt.

In the event the operation of the PFP is interrupted, aborted, or hangs up, the system may be reset in one of two ways. A software reset may be issued by the host, or a hardware reset may be issued by pressing the reset button on the PFP. The button is located on the center rack directly below the power switches. (See figure 3.1-1) The result is identical. The software command merely allows the user to reset the machine from a remote location. After the machine has been reset, the application must be re-loaded and re-started in order to run correctly.

3.2.4 Off-line Routine Procedures

The Intel 310 host requires no off-line routine procedures other than routine cleaning of the floppy disk drive and cartridge tape drive. See the Intel 310 Hardware User's Manual for instructions and maintenance intervals.

The PFP requires the the four air filters located on the front of the machine and the air filter located beneath the crossbar to be taken out and cleaned monthly (more often if the filters appear dirty).

3.2.5 Other Procedures

4. Diagnostic Procedures

4.1 Diagnostic Features Summary

The Intel 310 runs internal diagnostics on power up or system reset which test the processor subsytem, memory subsystem, and boot subsystem. Comprehensive diagnostic programs for the 310 are available from Intel in their iMDDX diagnostic package (order number 174032-001).

The iSBC 286/12 processors in the PFP each run their own diagnostics on power up or system reset. The processor and memory subsystems are tested similarly to the processor and memory in the host. While the test is running a red LED located on the front of the processor remains on. After the test is passed a green light comes on. The test runs approximately five seconds. If the red light remains on longer than this time, the processor has failed and should be replaced.

Comprehensive diagnostics for the PFP are stored on the host 310. Programs are available to test all major portions of the system including the Multibus repeater system, crossbar data paths, sequencer handshake cables, sequencer and crossbar memory, and the hardware assisted functions on the processor. Each test runs in an infinite loop until it is stopped at the host. Errors can be reported to a disk file or to the printer. Each test also has output to the system terminal to indicate the current state of the test while it is running.

4.2 Diagnostic Procedures

4.2.1 Basic Processor Functionality Test

The Basic Processor Functionality Test (named "blink" on the host) checks the individual processors, including their ability to access shared memory and execute code. The test cycles each processor through a series of 4 states. Each state on each processor is identified by the status of the LEDs on the front of the processor. (There are 4 different combinations of the LEDs that are used.) The processor state is sent to the host to be displayed at the user terminal. Output may be directed to a disk file by editing the "process.txt" file. (See the programmer's manual for a description of this file.)

In order to run the test, follow these steps:

1) Sign on the Intel 310 using the logon name "PFP" and the password "PFP".

2) Move to the directory "/test/blink".

3) Type "make run" to run the test. All of the processors that were loaded (see the process.txt file) will be tested. The terminal screen will come up with a display indicating that the test is running. The door to each processor rack can be opened in order to watch the LEDs blink as they are cycled through each state. The test will run in an infinite loop until it is manually stopped.

4) To stop the test, type a "control C" at the terminal.

4.2.2 Crossbar Network Transfer Test

The Crossbar Network Transfer Test (called "ntest") checks all data paths through both crossbar networks, the sequncer/crossbar interface, all processor/crossbar interfaces, and associated cabling. Each processor takes a turn broadcasting a data word to the other 31 processors on the network. Each recieving processor knows what the correct value should be, so any discrepancies are reported to the host to be displayed at the terminal. Sixty-four different patterns are used in succession. The test will run in a continuous loop until it is stopped manually. Test results may be sent to a disk file by editing the "process.txt" file. (See the programmer's reference manual for a description of this file.)

In order to run the test, follow these steps:

1) Sign on the Intel 310 using the logon name "PFP" and the password "PFP".

2) Move to the directory "/test/ntest".

3) Type "make run" to run the test. The terminal screen will periodically update the number of crossbar cycles completed, indicating that the test is running. The test will run in an infinite loop until it is manually stopped.

4) To stop the test, type a "control C" at the terminal.

In order to run the test on a specific set of processors, edit the "process.txt" file accordingly.

4.2.3 System Memory Test

The System Memory Test checks the master Multibus repeater located in the host, the slave repeaters located in each processor rack, the Multibus backplanes located in each processor rack, the Multibus interface on each processor, and the associated cabling. The host writes random data to all processor, crossbar, and sequencer memory locations and then reads them back for verification. (The lowest 4096 bytes of each processor cannot be tested.) The test will run once and stop. Test results may be sent to the disk file "error.log". The test may be run on any processor, sequencer, or crossbar individually, or as a complete system.

In order to run the test on the complete system, follow these steps:

1) Sign on the Intel 310 using the logon name "PFP" and the password "PFP".

2) Move to the directory "/test/mtest".

3) Type "submit all" to run the test on the full system. The terminal screen will come up with a display indicating that the test is running.

To run the test on an individual component, enter the following commands:

1) Sign on the Intel 310 using the logon name "PFP" and the password "PFP".

2) Type "mtest" for a brief description of the normal usage. The first command line parameter is the name of the component to be tested. The second parameter is the starting (offset) address which must be at least 1000 (hexadecimal) for any processor. The third parameter is the length od the memory region to be tested. The sum of "length" and "offset" must be less than or equal to the number of bytes available on that component. (See the ENVIRONMENT file on the :home: directory.) to run the test on an individual component.The terminal screen will come up with a prompt asking for the component's ⟨name⟩, ⟨offset⟩, and ⟨length⟩. Valid processor names are P0 through P63. Valid sequencer and crossbar names are S1, S2, X1, and X2 respectively.

4) To stop the test, type a "control C" at the terminal.

4.2.4 Hardware Assisted Function Test

Special "piggyback" boards are available to speed the calculations of certain functions through the use of hardware. Exponentials, square roots, natural logarithms, reciprocals, sines, cosines, tangents, arcsines, arccosines, and arctangents are all supported. This test has each processor compute each function over a given range and then compares the answers from each processor to known values stored at the host. At the present time, this test only supports the GT-FPP/3 processor. The test will run in a continuous loop until it is stopped manually. Test results may be sent to the printer or a disk file.

In order to run the test, follow these steps:

1) Sign on the Intel 310 using the logon name "PFP" and the password "PFP".

2) Move to the directory "/test/function".

3) Type "submit function" to run the test. The terminal screen will come up with a display indicating that the test is running. The test will run in an infinite loop until it is manually stopped.

4) To stop the test, type a "control C" at the terminal.

4.3 Diagnostic Tools

4.3.1 Digital Oscilliscope

A Hewlett-Packard digitizing oscilliscope, model 54201D, or equivalent is recommended for on-site debugging of problems encountered when running system diagnostics.

4.3.2 Digital Multimeter

A Fluke digital Multimeter, model 77, or equivalent is reccomended for on-site debugging of problems encountered when running system diagnostics.

4.3.3 Logic Analyzer

An NWIS Microanalyst logic analyser, model 2200 , or equivalent, is reccomended for on-site debugging of problems encountered when running system diagnostics.

5 Notes

5.1 Acronym Glossary

1.CSOM - Computer System Operator's Manual

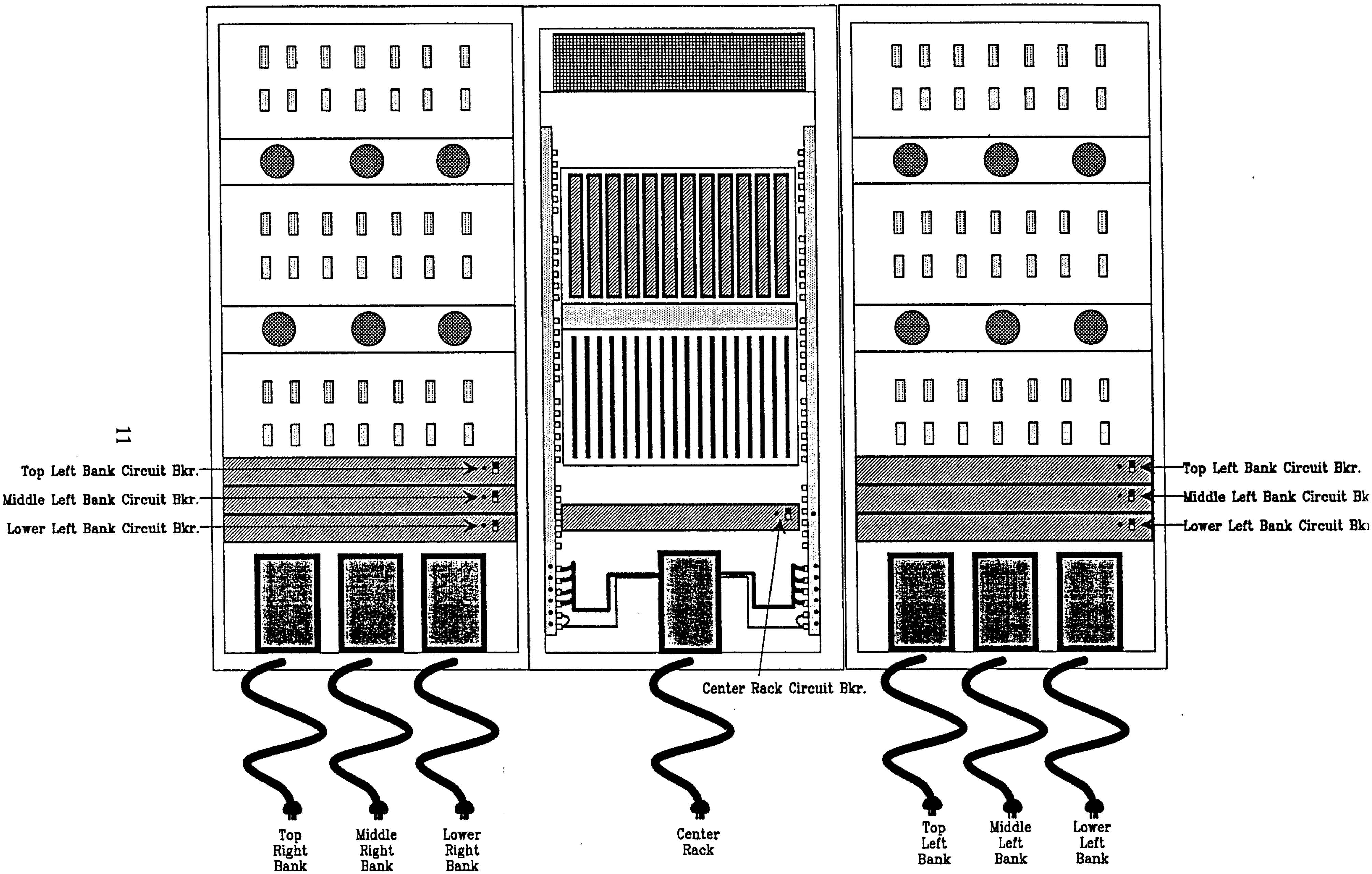
2. LED - Light Emitting Diode

3. PFP - Parallel Function Processor

Appendix A Figures

Figure 3.1-1 Location of Power Switches

Figure 3.1-2 Location of Ckt Breakers & Pwr Cables



(Rear view of system)

Figure 3.1-1 Location of Circuit Breakers and Power Cables

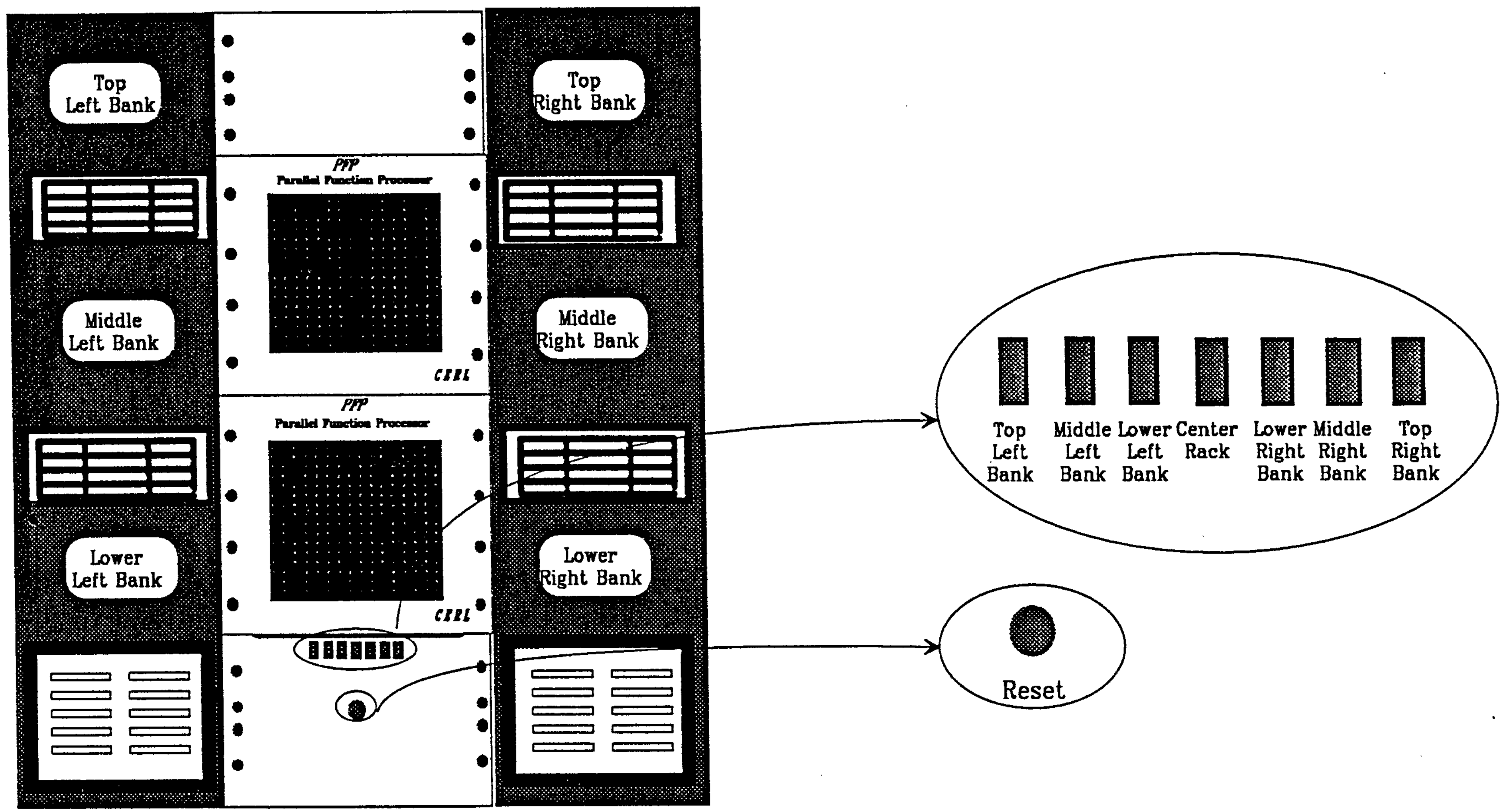


Figure 3.1–2 Location of Power Switches

Appendix B Debug Examples Using PFP Displays

There are 5 major steps involved in a crossbar transfer. They are:

1. The sequencer must set the appropriate data transfer paths in the crossbar. The paths being used can be identified by reading the crossbar display.

2. The sequencer asserts ROT/ (read out) on all processors that are sending data on that cycle.

3. The Sequencer waits to see DAV/ (data available) from all sending processors and RFI/ (ready for input) on all processors receiving on that cycle. Status lines from processors not involved in that cycle are ignored.

4.The sequencer asserts WIN/ on all receiving processors.

5. The sequencer negates the active ROT/ and WIN/ lines to terminate the cycle.

Example 1 Two Sends Each With Multiple Receivers

Example 1 has processor P1 sending to processors P16, P18, P19, and P21 while processor P23 sends to P0, P4, and P8.

The five transfer steps are shown on the next 5 figures. They are:

1. The sequencer sets up the crossbar data paths.

2. The sequencer asserts ROT/ on the sending processors (P1 and P23).

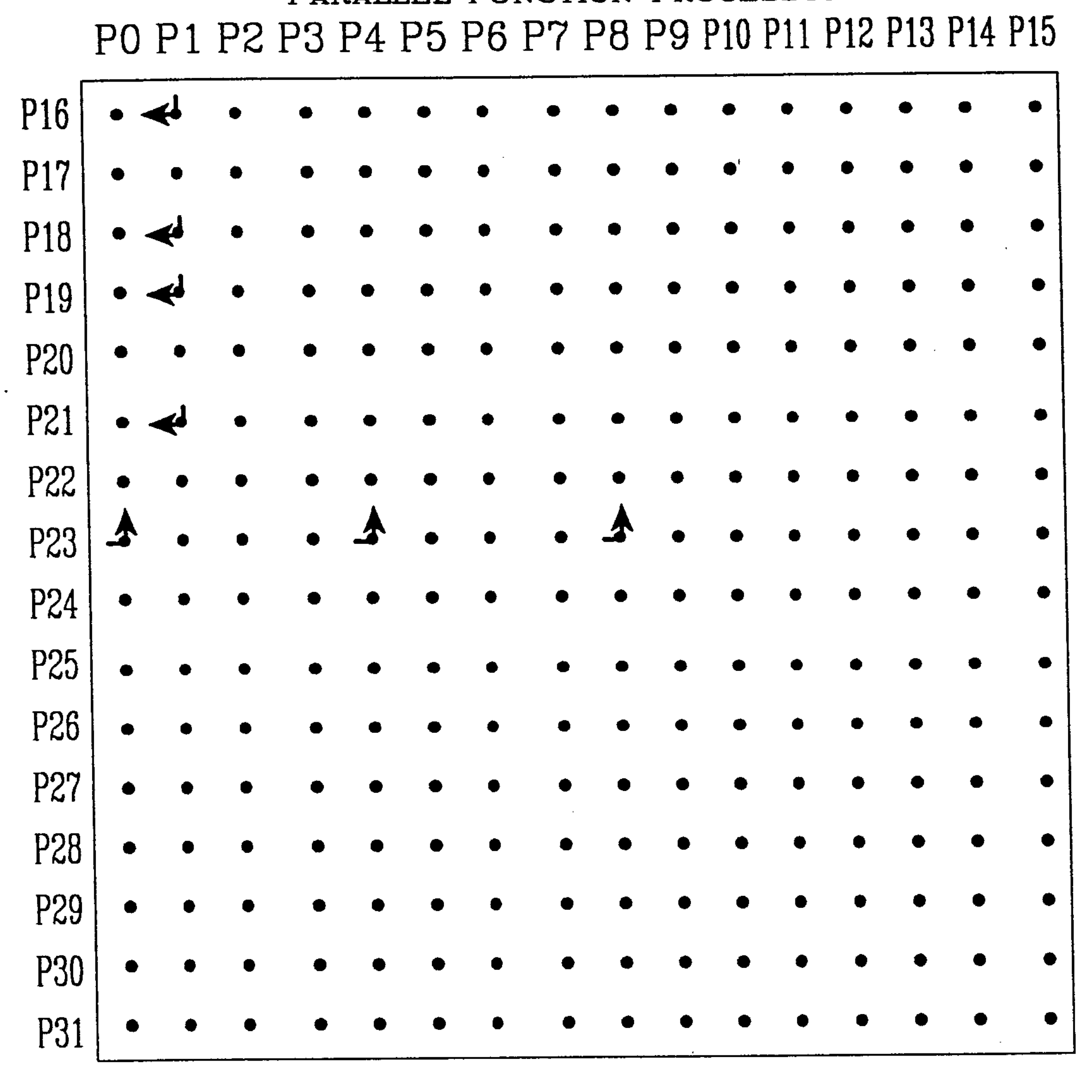
3. The Sequencer waits to see DAV/ (data available) from all sending processors (P1 and P23) and RFI/ (ready for input) on all processors receiving on that cycle (P0, P4, P8, P16, P18, P19, and P21). Status lines from processors not involved in that cycle are ignored.

4.The sequencer asserts WIN/ on all receiving processors (P0, P4, P8, P16, P18, P19, and P21).

5. The sequencer negates the active ROT/ (P1 and P23) and WIN/ (P0, P4, P8, P16, P18, P19, and P21) lines to terminate the cycle.

PFP

PARALLEL FUNCTION PROCESSOR



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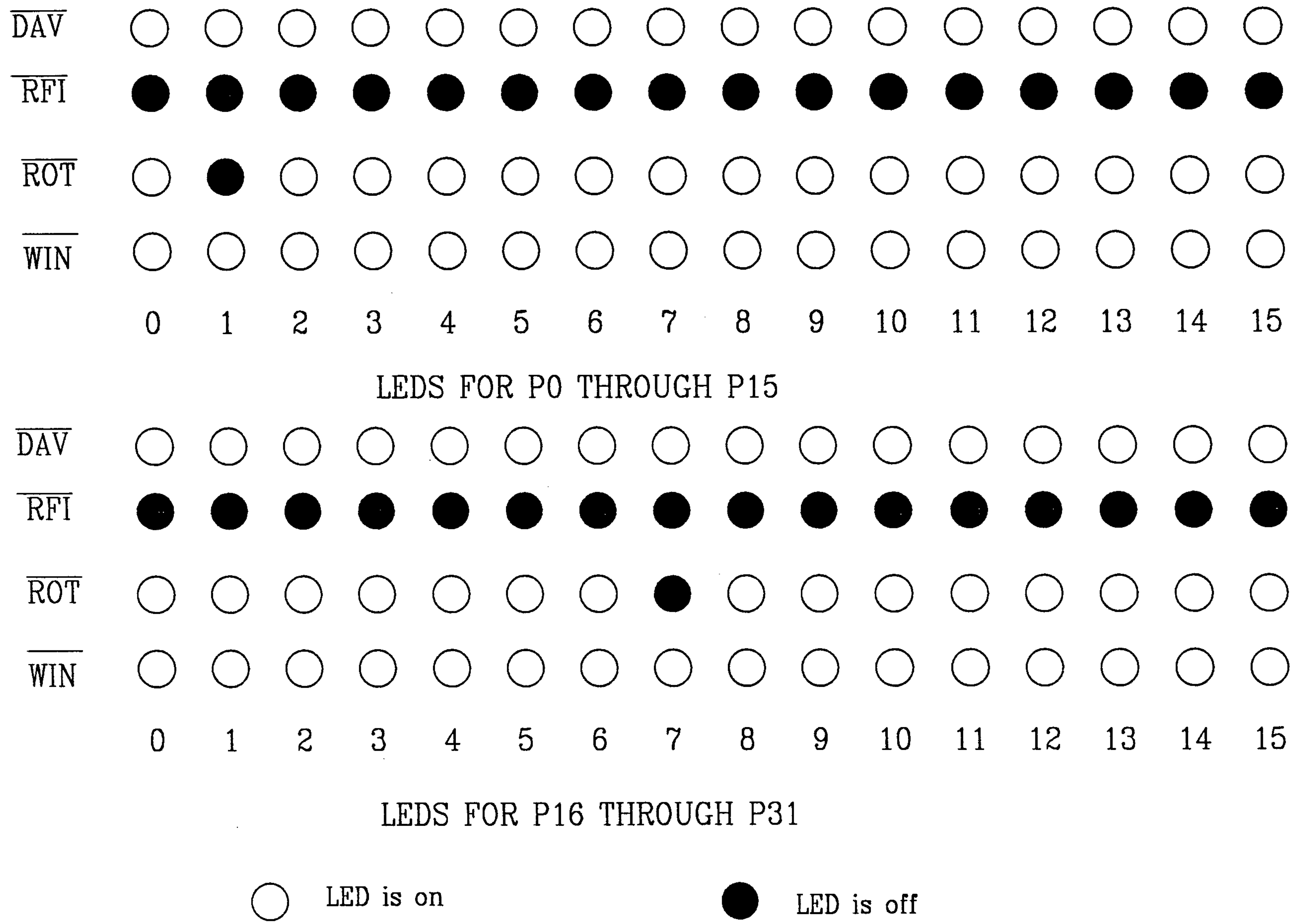
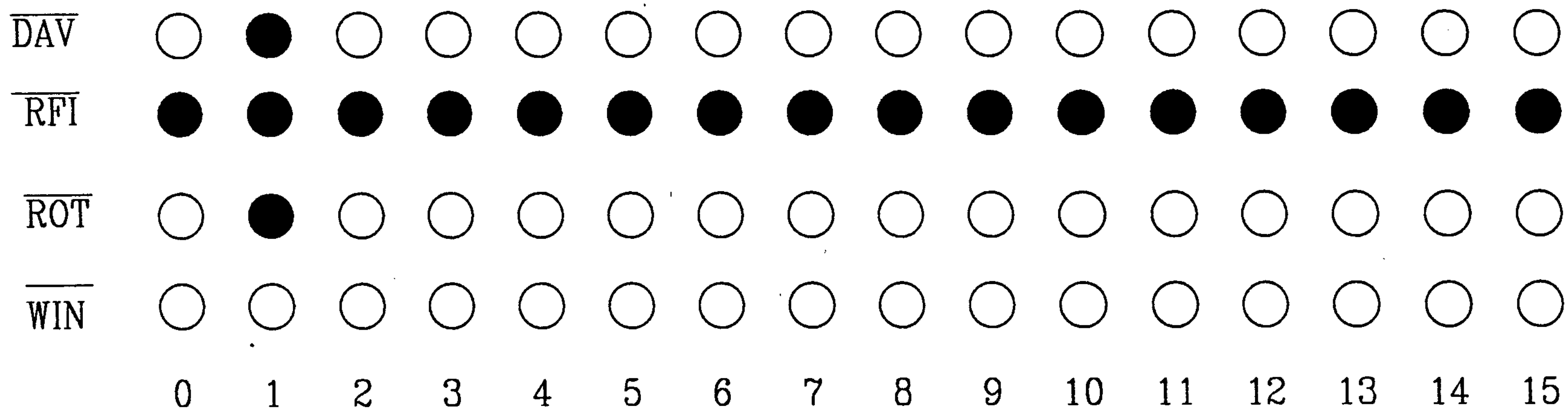
CYCLE

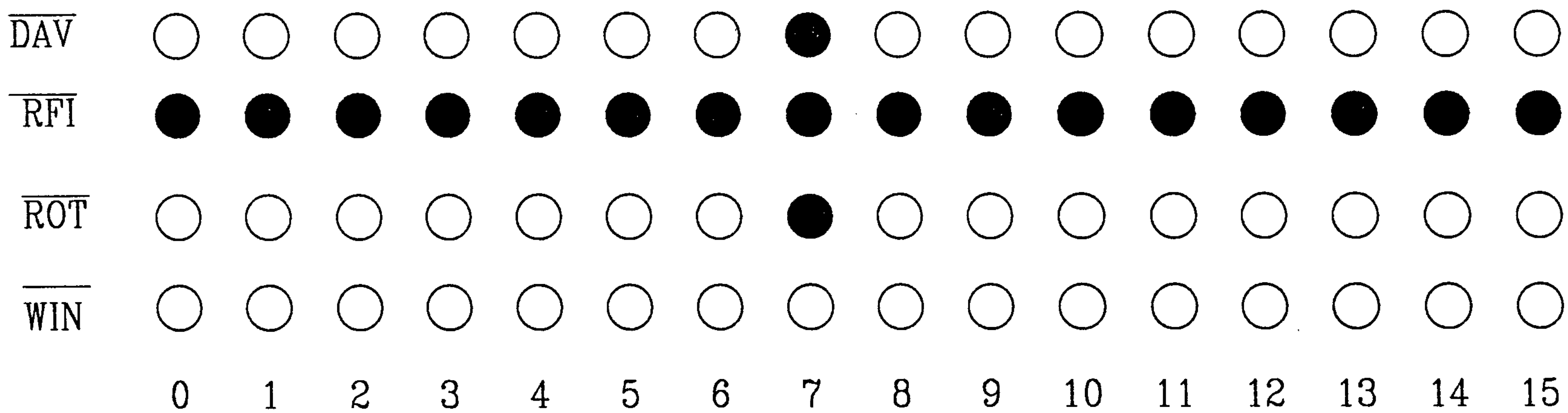
P16,P18,P19,P21 := P1
P0,P4,P8 := P23



Example 1 Step 2



LEDS FOR P0 THROUGH P15



LEDS FOR P16 THROUGH P31

○ LED is on ● LED is off

Example 1 Step 3

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$\overline{DAV}$	○	●	○	○	○	○	○	○	○	○	○	○	○	○	○	○
$\overline{RFI}$	○	●	●	●	○	●	●	●	○	●	●	●	●	●	●	●
$\overline{ROT}$	○	●	○	○	○	○	○	○	○	○	○	○	○	○	○	○
$\overline{WIN}$	●	○	○	○	●	○	○	○	●	○	○	○	○	○	○	○

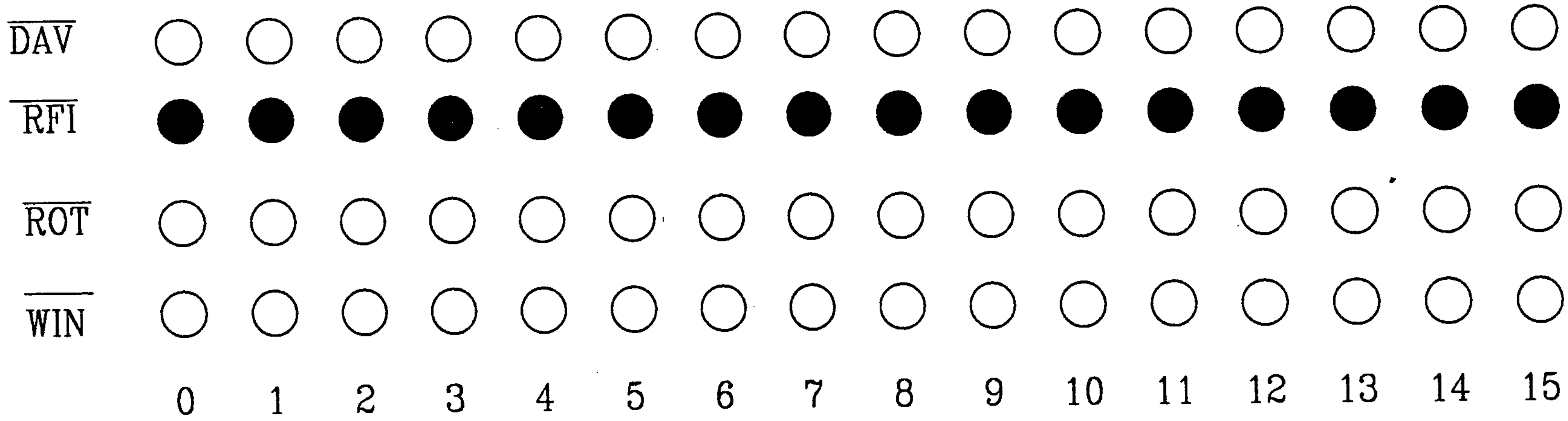
LEDS FOR P0 THROUGH P15

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$\overline{DAV}$	○	○	○	○	○	○	○	●	○	○	○	○	○	○	○	○
$\overline{RFI}$	○	●	○	○	●	○	●	●	●	●	●	●	●	●	●	●
$\overline{ROT}$	○	○	○	○	○	○	○	●	○	○	○	○	○	○	○	○
$\overline{WIN}$	●	○	●	●	○	●	○	○	○	○	○	○	○	○	○	○

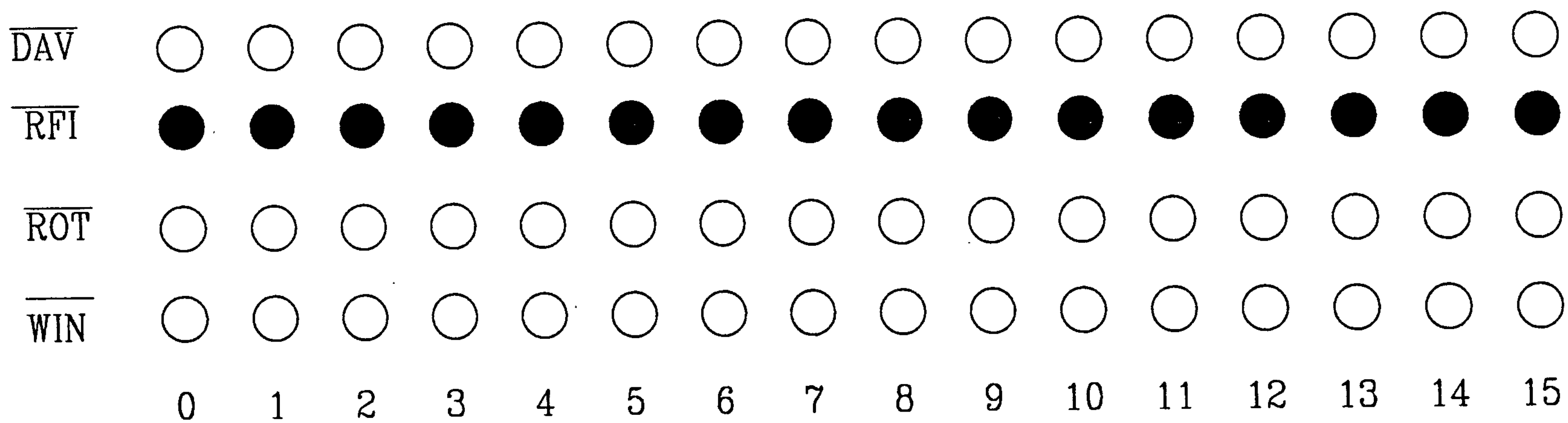
LEDS FOR P16 THROUGH P31

○ LED is on ● LED is off

Example 1 Step 4



LEDS FOR P0 THROUGH P15



LEDS FOR P16 THROUGH P31

Example 1 Step 5

Example 2 One Processor Broadcasting to 31 Others

Example 2 shows processor P17 broadcasting a data word to the other 31 processors on the crossbar. All 31 receive the same word at the same time.

The five transfer steps are shown on the next 5 figures. They are:

1. The sequencer sets up the crossbar data paths.

2. The sequencer asserts ROT/ on the sending processor (P17).

3. The Sequencer waits to see DAV/ (data available) from all sending processors (P17) and RFI/ (ready for input) on all processors receiving on that cycle (all others).

4.The sequencer asserts WIN/ on all receiving processors (all but P17).

5. The sequencer negates the active ROT/ (P17)and WIN/ (all others) lines to terminate the cycle.

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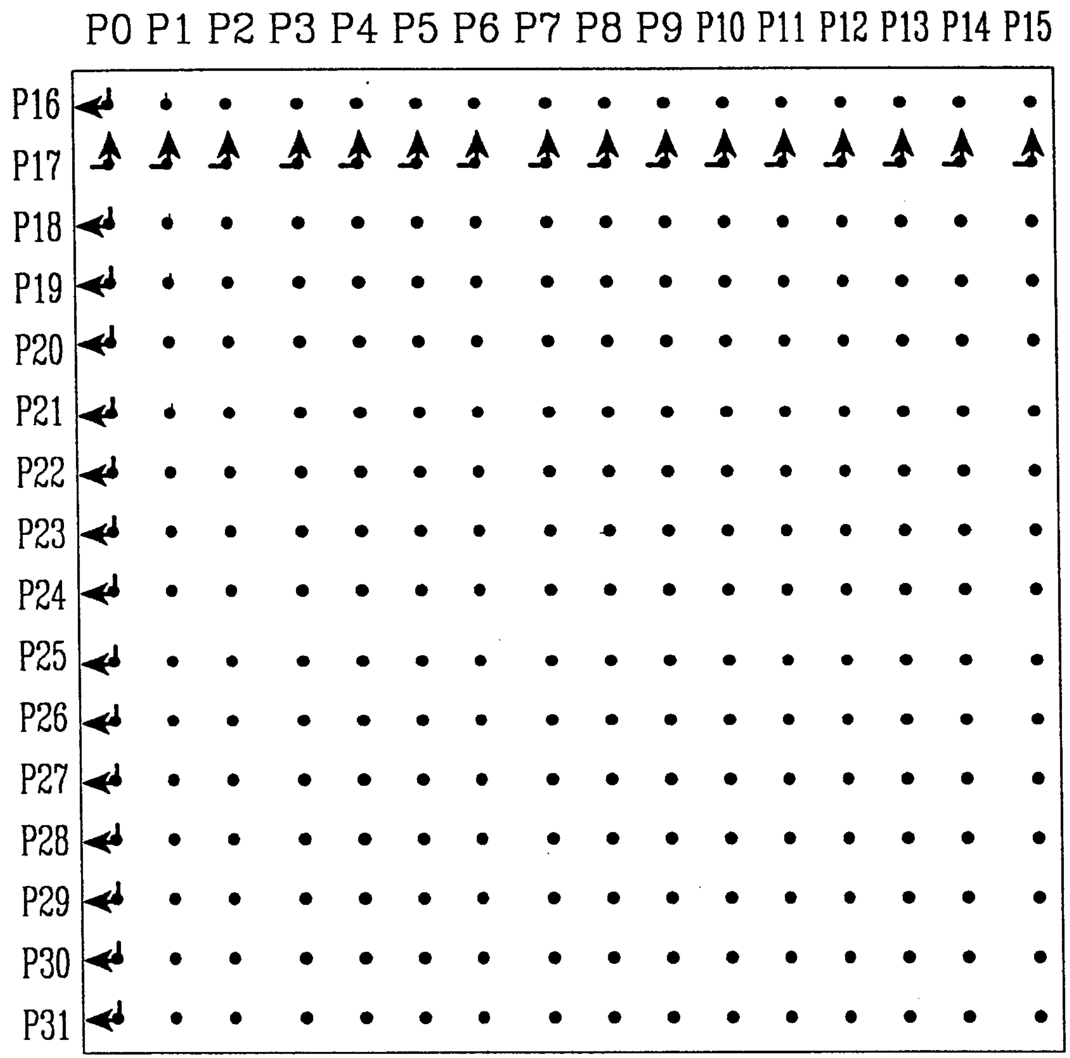

CYCLE

P0,P1,P2,P3,P4,P5,P6,P7,P8,
P9,P10,P11,P12,P13,P14,P15,
P16,P18,P19,P20,P21,P22,P23,P24,
P25,P26,P27,P28,P29,P30,P31:=P17

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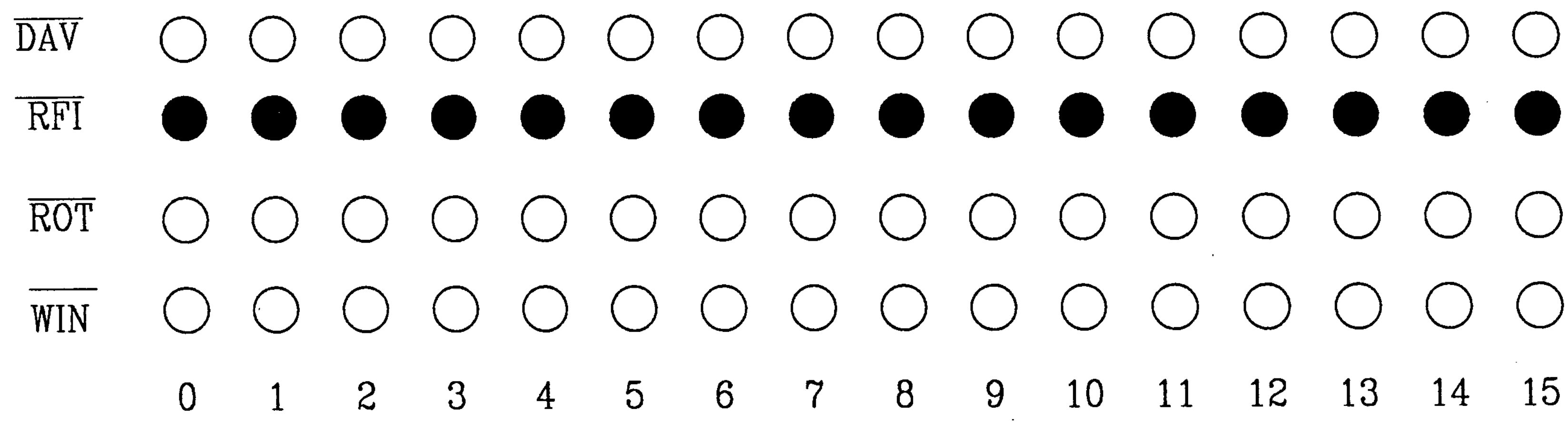
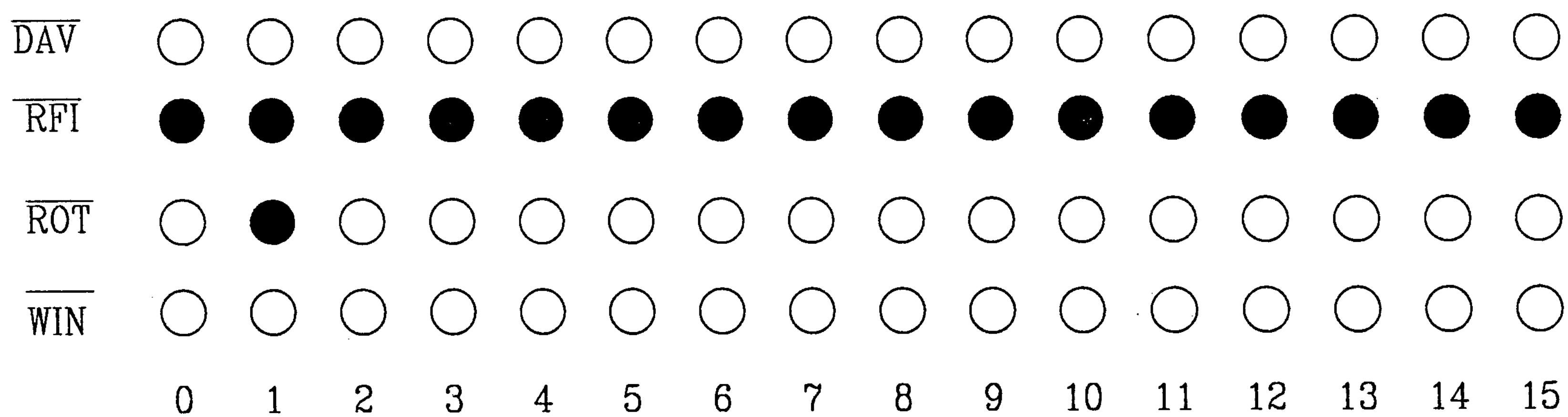
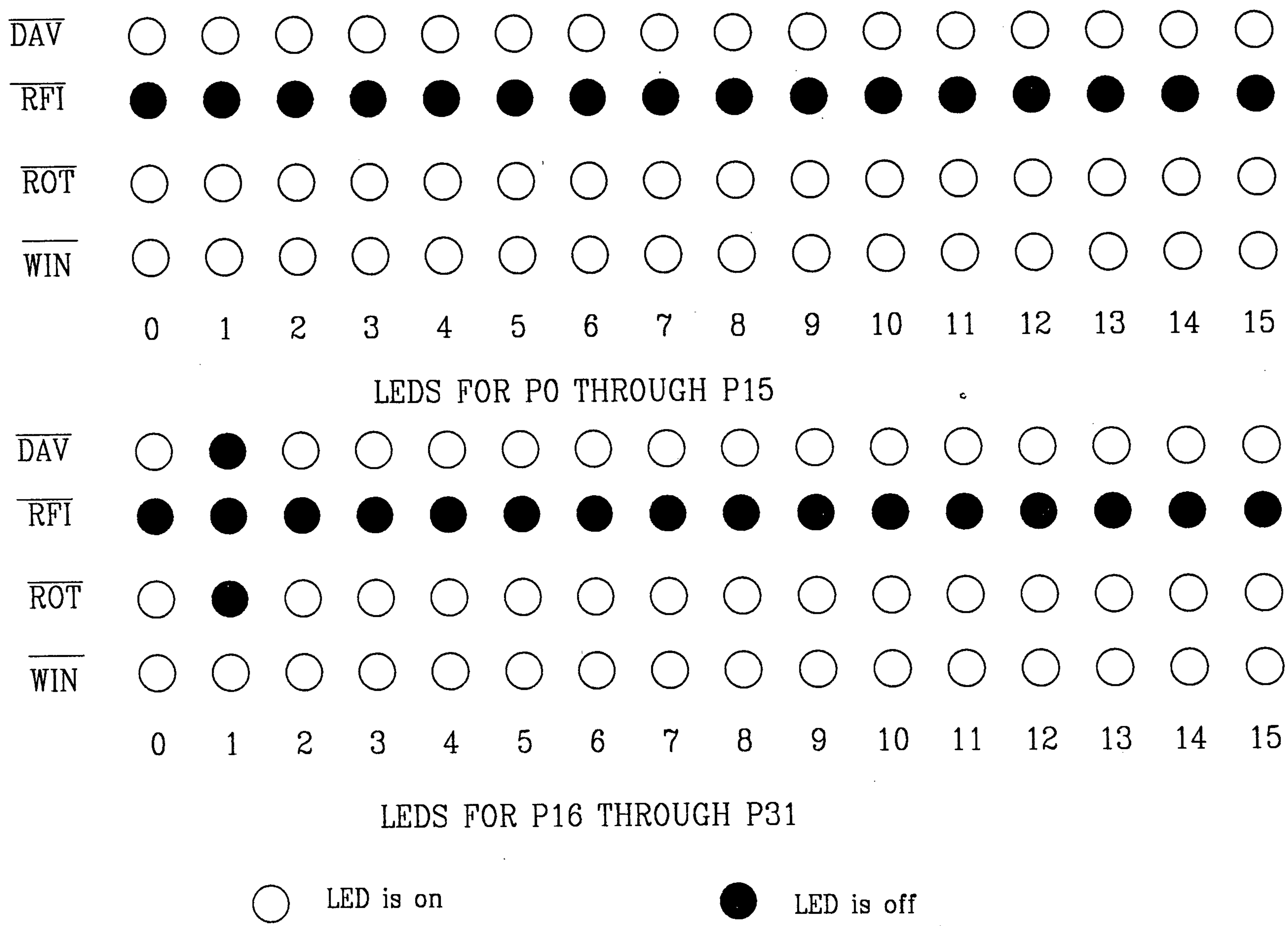


LEDS FOR P0 THROUGH P15

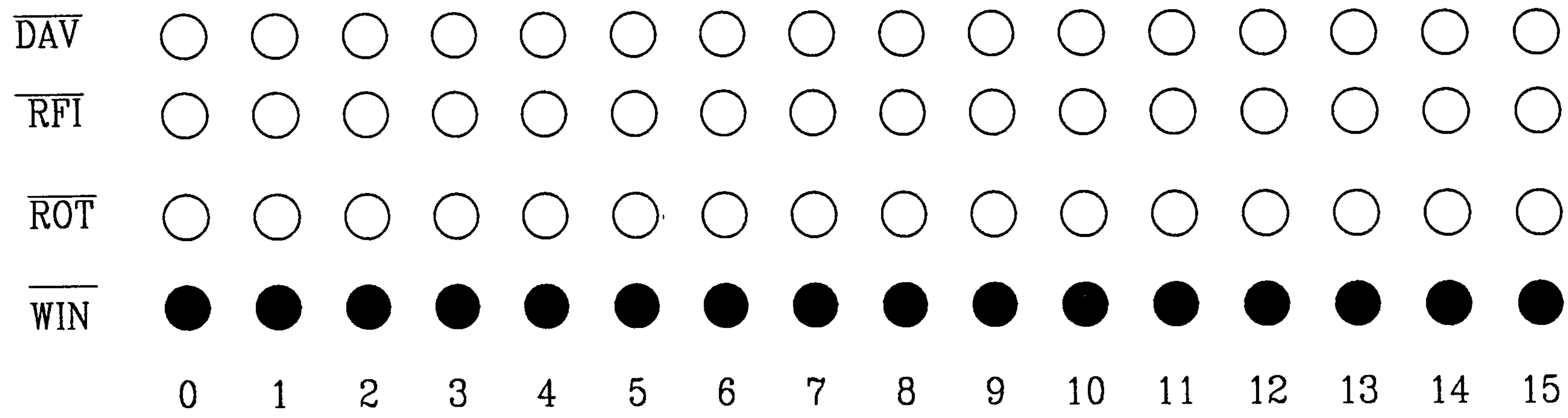


LEDS FOR P16 THROUGH P31

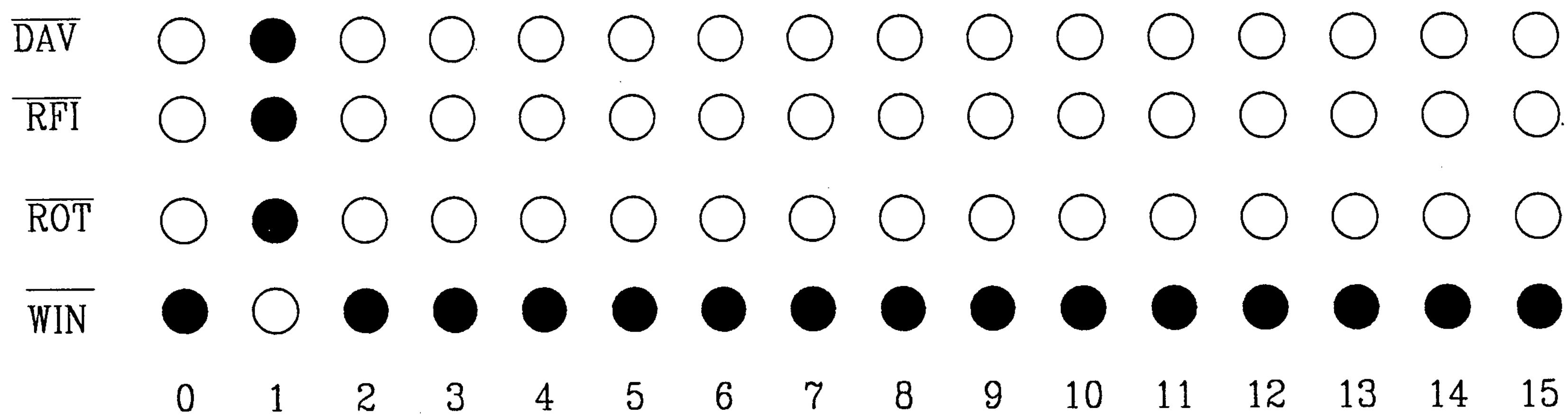
Example 2 Step 2



Example 2 Step 3

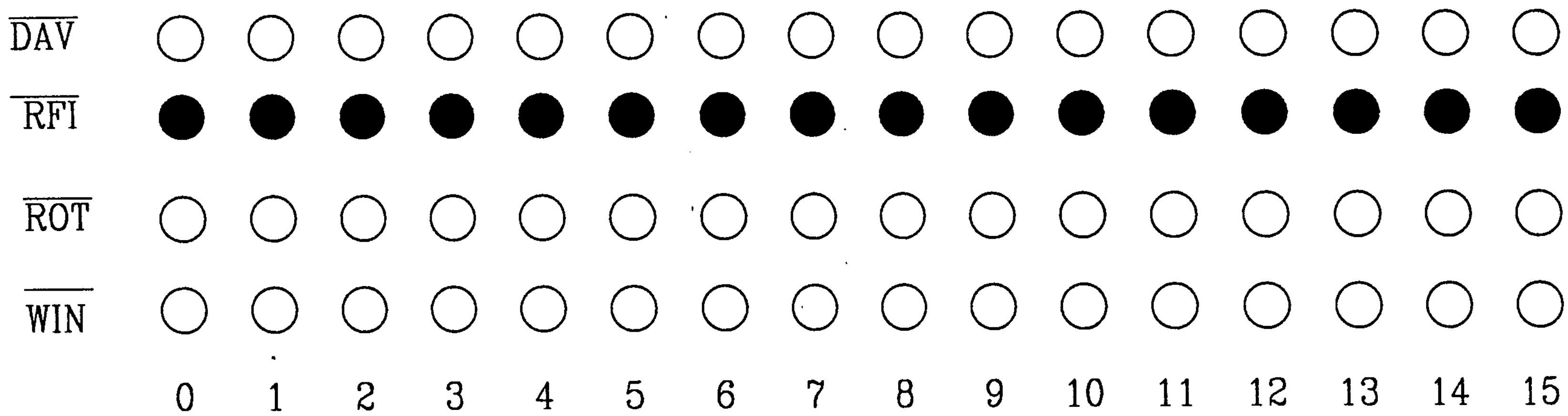


LEDS FOR P0 THROUGH P15

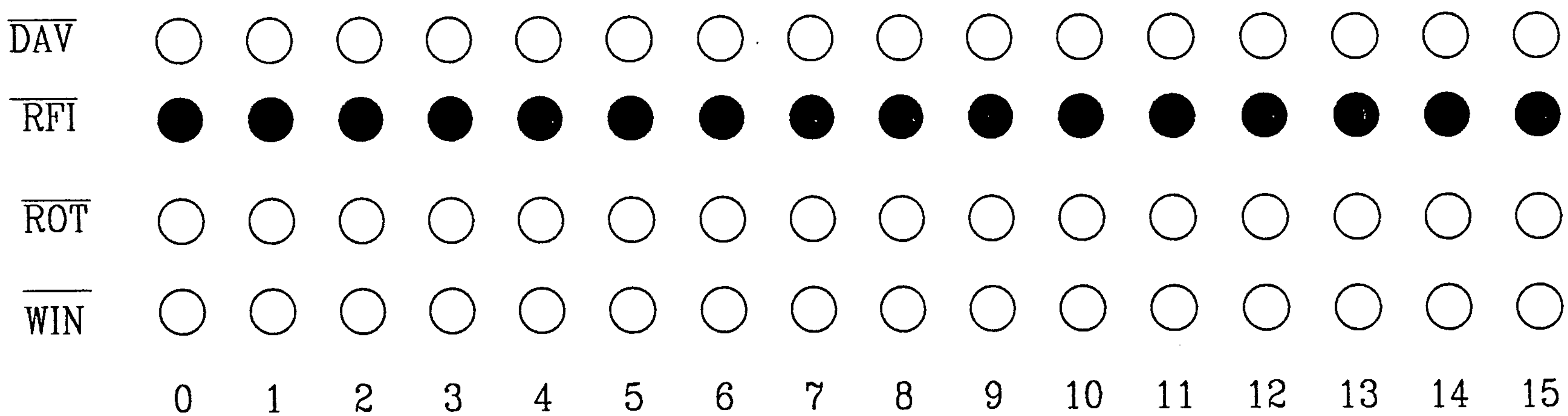


LEDS FOR P16 THROUGH P31

Example 3 Step 4



LEDS FOR P0 THROUGH P15



LEDS FOR P16 THROUGH P31

Example 2 Step 5

Example 3 Five Simultaneous Sends With Multiple Receives

Example 3 shows processor P5 sending to processors P25, P26, P27, and P28, while processor P2 sends to P24, processor P23 sends to P3, processor P22 sends to P21, and processor P12 sends to P7, P10, and P15.

The five transfer steps are shown on the next 5 figures. They are:

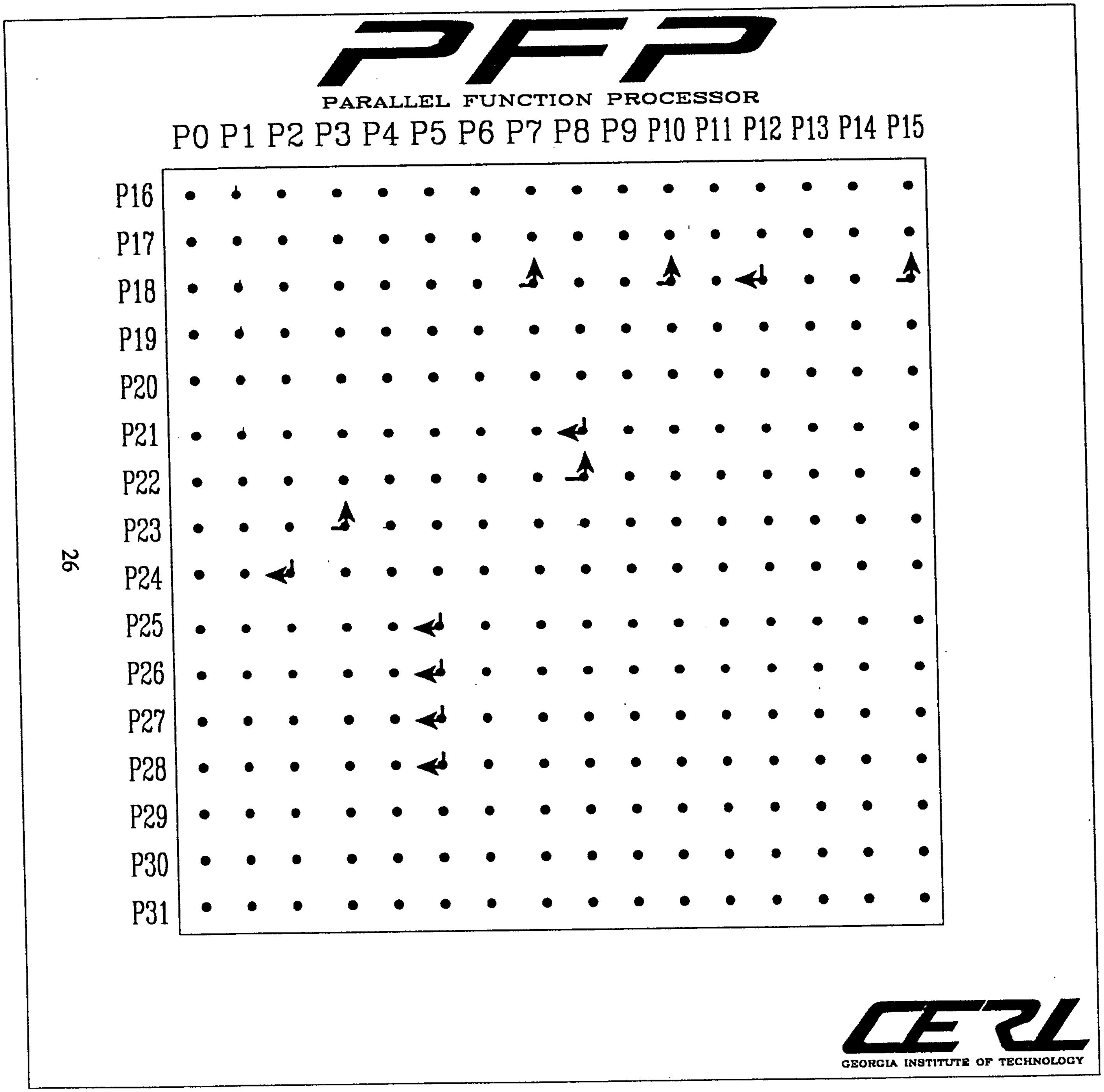
1. The sequencer sets up the crossbar data paths.

2. The sequencer asserts ROT/ on the sending processors (P2, P5, P22, P23, and P12).

3. The Sequencer waits to see DAV/ (data available) from all sending processors (P2, P5, P22, P23, and P12) and RFI/ (ready for input) on all processors receiving on that cycle (P3, P7, P10, P15, P21, P24, P25, P26, P27, and P28).

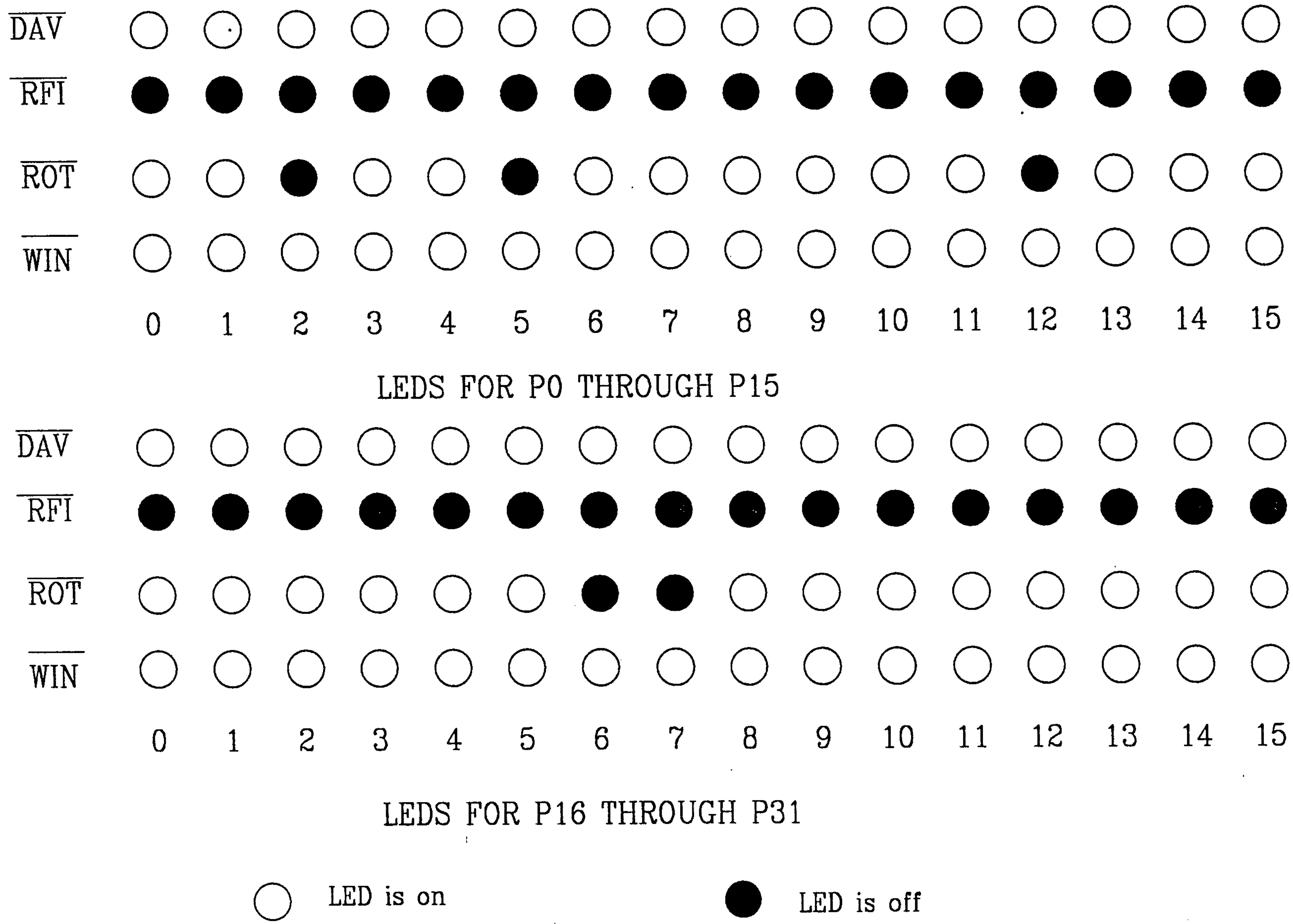
4.The sequencer asserts WIN/ on all receiving processors (P3, P7, P10, P15, P21, P24, P25, P26, P27, and P28).

5. The sequencer negates the active ROT/ (P2, P5, P22, P23, and P12) and WIN/ (P3, P7, P10, P15, P21, P24, P25, P26, P27, and P28) lines to terminate the cycle.

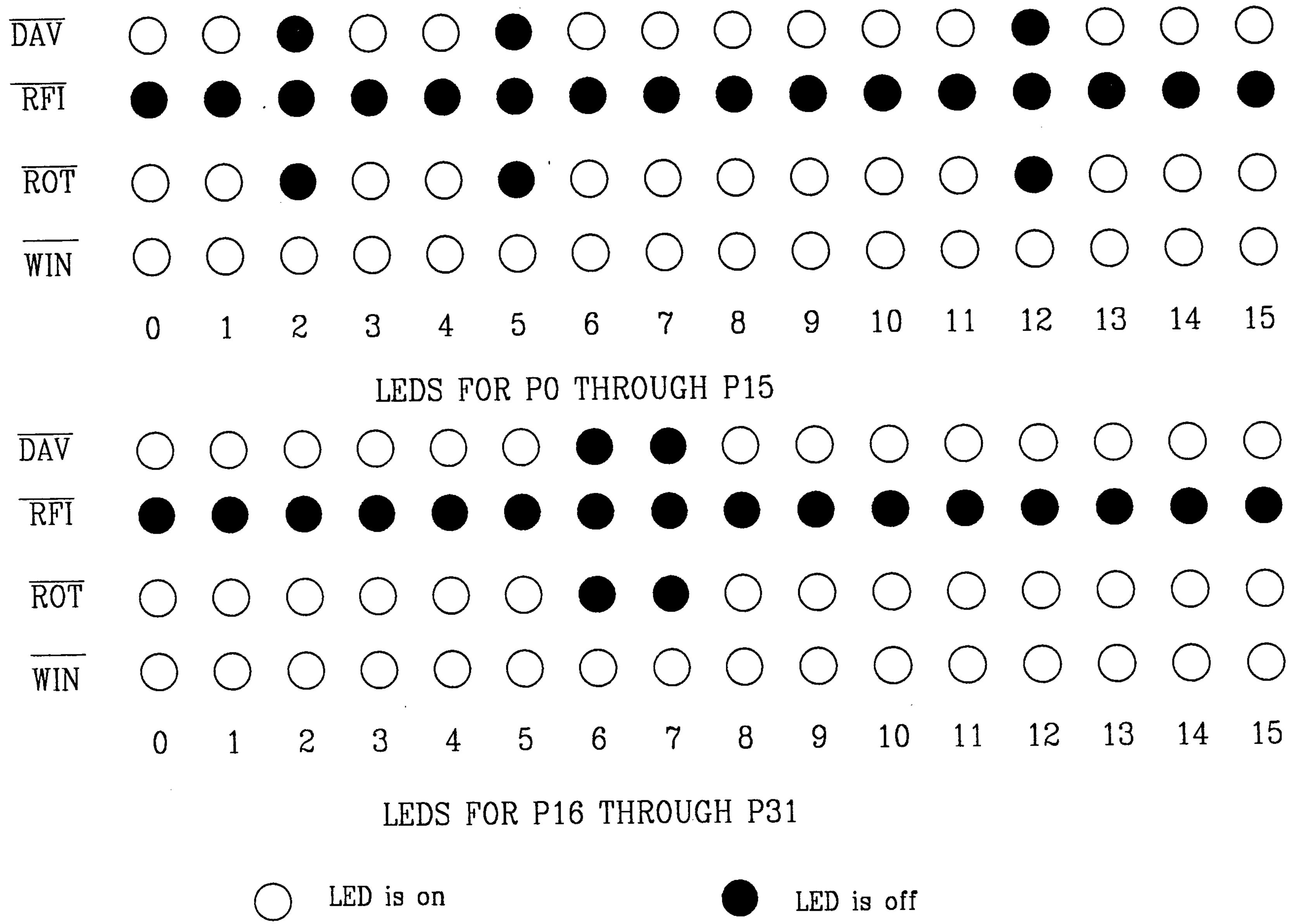


CYCLE

P25,P26,P27,P28 := P5
P24 := P2
P3 := P23
P21 := P22
P7,P10,P15 := P12



Example 3 Step 2



Example 3 Step 3

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$\overline{DAV}$	○	○	●	○	○	●	○	○	○	○	○	○	●	○	○	○
$\overline{RFI}$	●	●	●	○	●	●	●	○	●	●	○	●	●	●	●	○
$\overline{ROT}$	○	○	●	○	○	●	○	○	○	○	○	○	●	○	○	○
$\overline{WIN}$	○	○	○	●	○	○	○	●	○	○	●	○	○	○	○	●

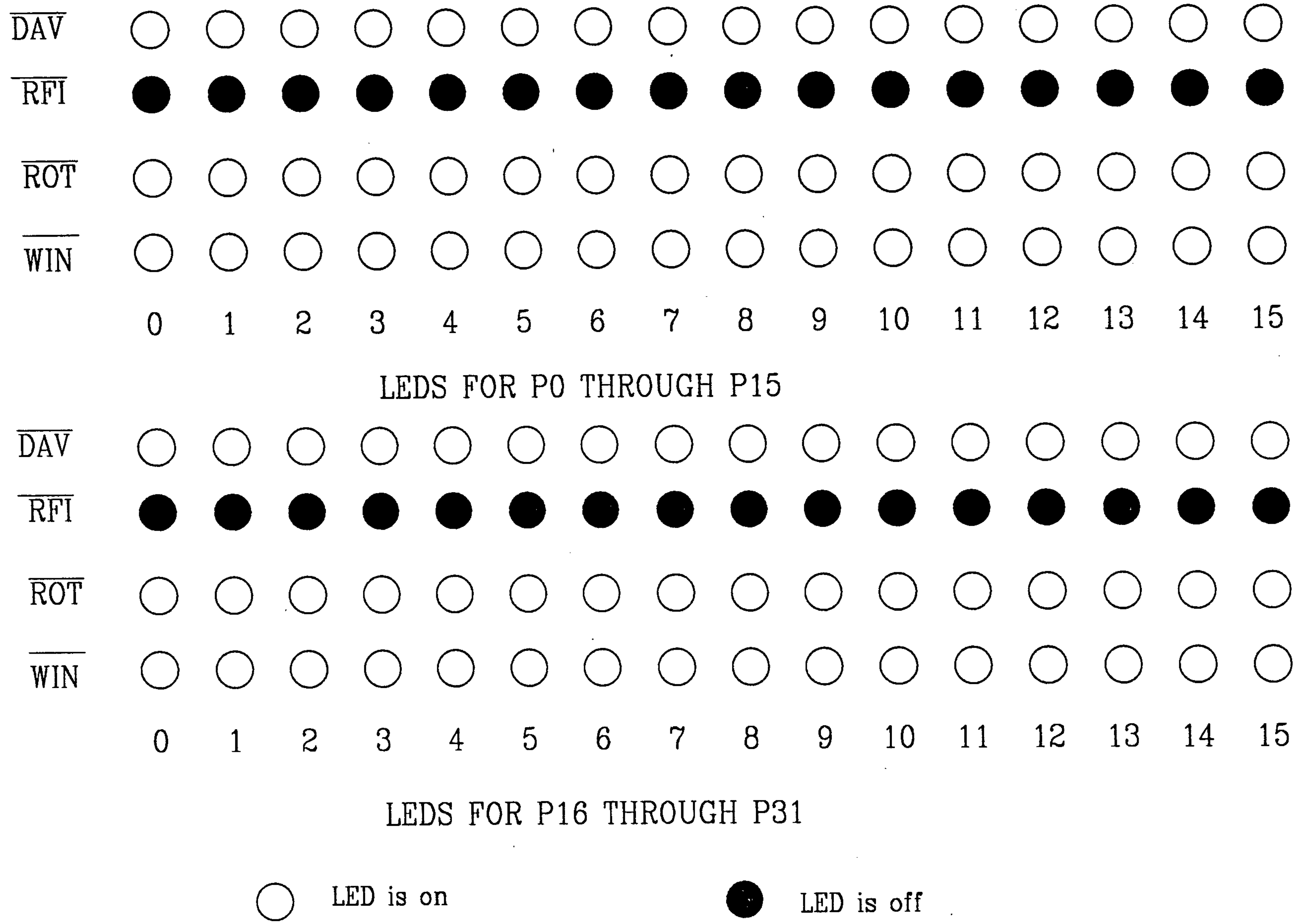
LEDS FOR P0 THROUGH P15

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$\overline{DAV}$	○	○	○	○	○	○	●	●	○	○	○	○	○	○	○	○
$\overline{RFI}$	●	●	●	●	●	○	●	●	○	○	○	○	○	●	●	●
$\overline{ROT}$	○	○	○	○	○	○	●	●	○	○	○	○	○	○	○	○
$\overline{WIN}$	○	○	○	○	○	●	○	○	●	●	●	●	●	○	○	○

LEDS FOR P16 THROUGH P31

○ LED is on ● LED is off

Example 3 Step 4



Example 3 Step 5